

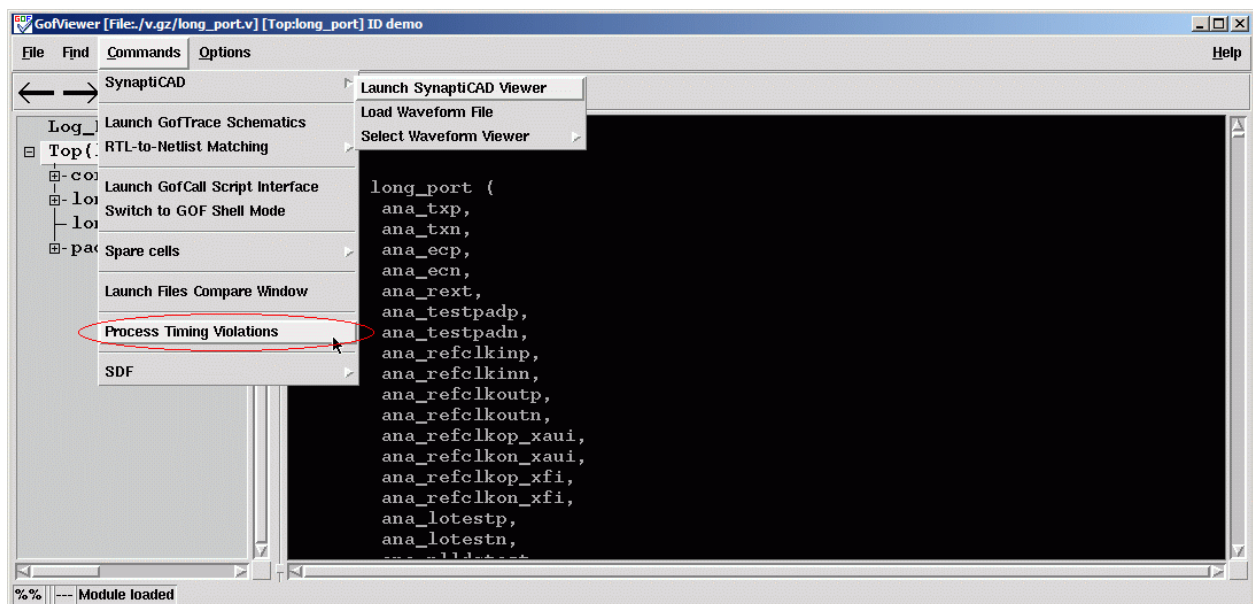
Timing Path Analysis by using Gates On the Fly

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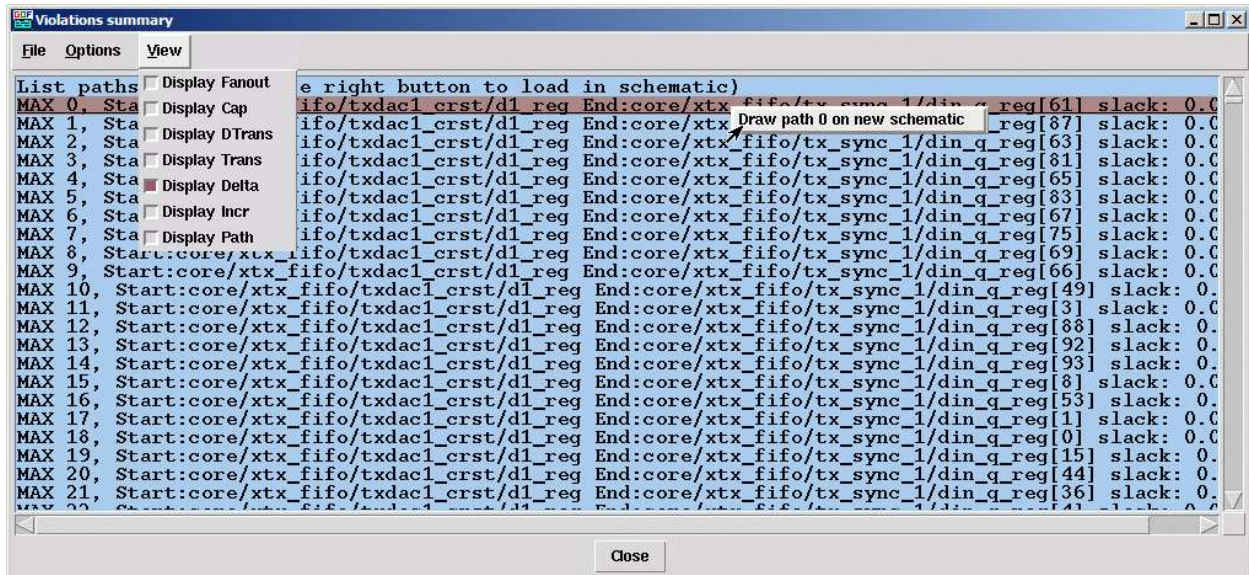
Getting started

- Load the library file, netlist and lef/def files
- `gof-lib tsmc.lib netlist.v -lef all_leaf.lef -def design.def`
- `-lef` and `-def` are optional. Layout view will not work if they are not present
- In GofViewer, select menu Commands -> 'Process Timing Violations'
- Pick the Prime Time violation report file, and run the command
- The time report command has typically these settings
- Report : timing
- `-path_type full_clock_expanded`
- `-delay_type max`
- `-input_pins`
- `-nets`
- `-max_paths 150`
- `-transition_time`
- `-capacitance`
- `-crosstalk_delta`



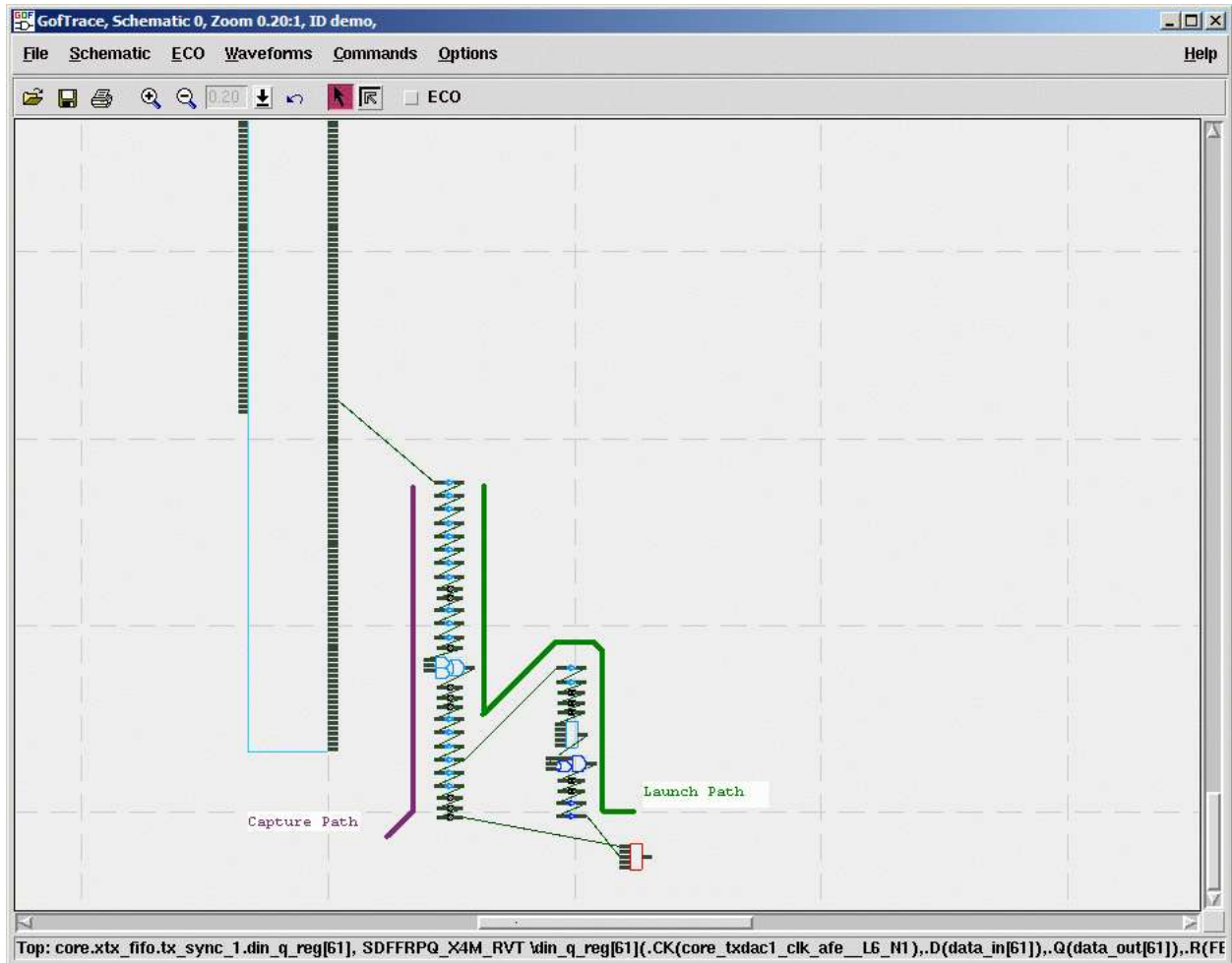
Process Prime Time report file

- Violation summary window pops up after report file parsed
- Select which item to be viewed on schematic
- Mouse left-button click one line to select the line
- Mouse right-button click to pop up menu to select 'Draw' command



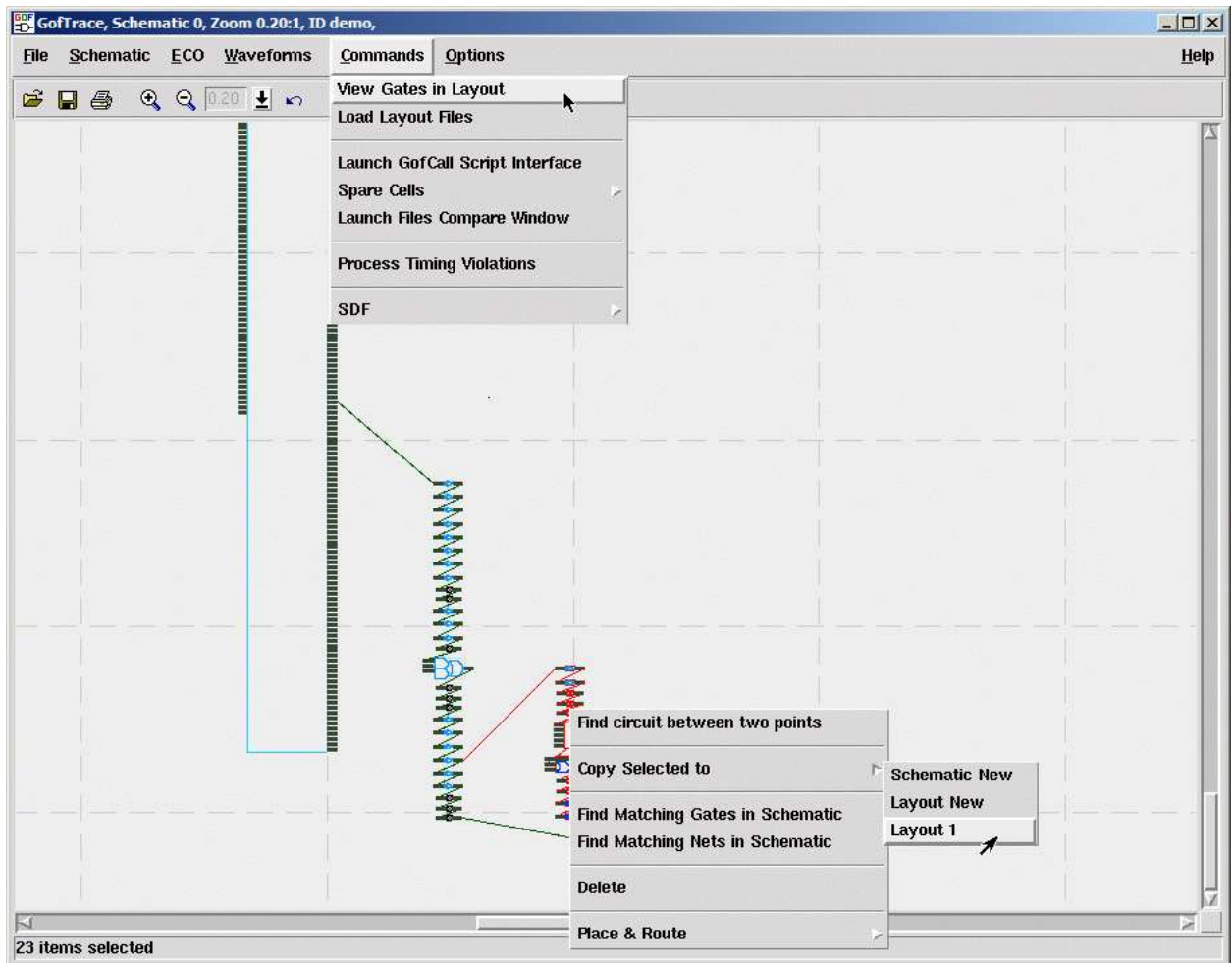
Analyze path on schematic

- Zoom out the schematic to get whole view
- The launch path and capture path are drawn side by side on the schematic
- In 40 nm, 'full_clock_expanded' is required for cross-talk in clock tree analysis
- The clock path maybe very long in large design



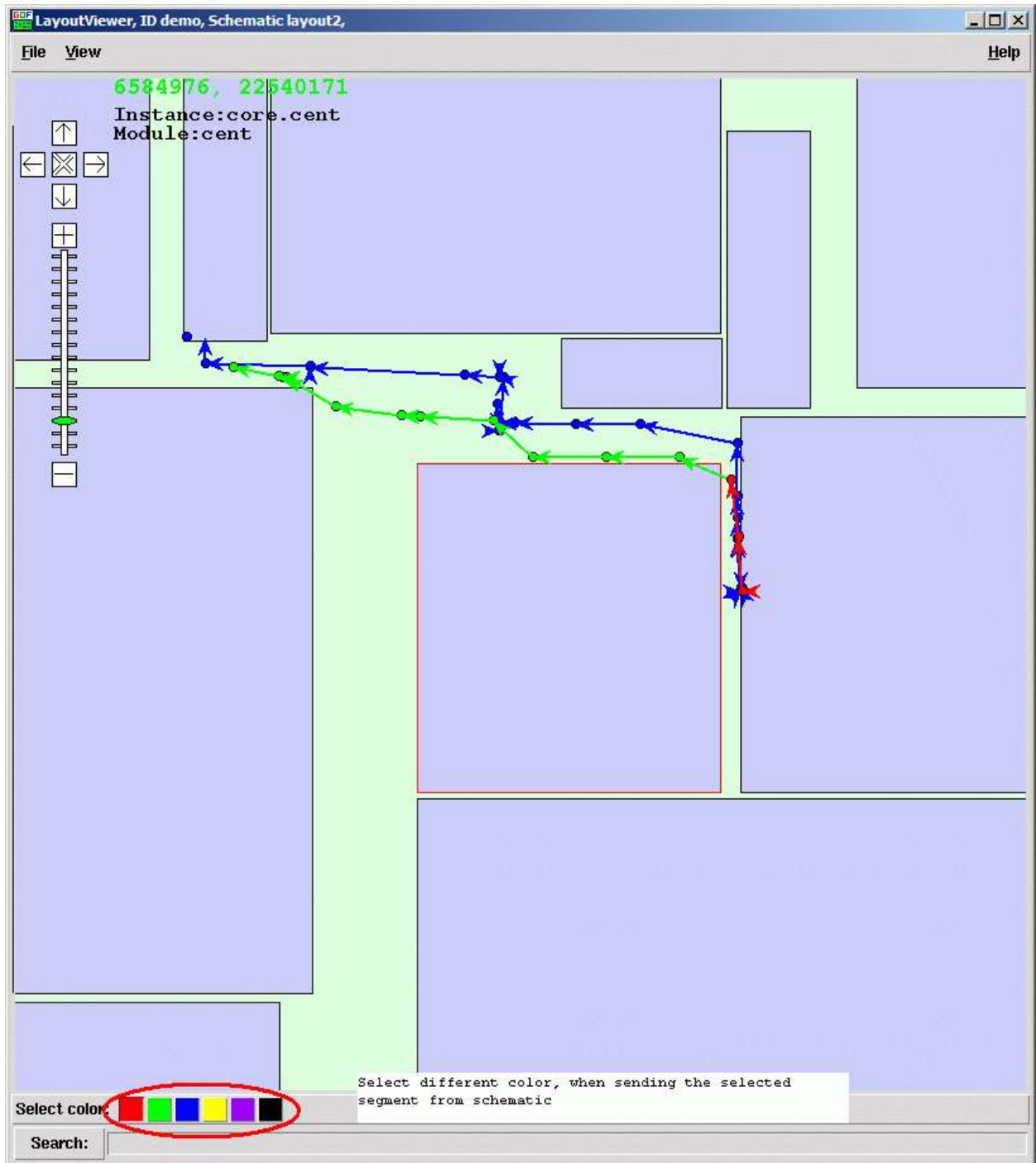
Interactivity

- Select a segment of schematic, launch path for example
- Choose menu Commands->'View Gates in Layout'
- Or pop menu, 'Copy Selected to'-'Layout #'



Gates On the Fly Use Case: Timing Path Analysis

- In layout view window, select different color
- Choose other segment of the schematic, capture path for example
- Copy selected to the same layout view again



Gates On the Fly Use Case: Timing Path Analysis

- Any gate selected on the layout view window can be sent back to the existing schematic or new schematic
- Any selected gates and connections can be sent to the layout view by drag&drop or menu operation

